forming a first pull-up transistor within the first semiconductor structure by forming a first source, a first drain and a first gate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source, a second drain, and a second gate;

forming a first contact and a second contact within the first semiconductor structure;

coupling the first drain to the second drain;

coupling the first gate to the second gate; and

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure.

79. A method of fabricating a memory device:

forming a first semiconductor structure and a second semiconductor structure;

forming a first pull-up transistor within the first semiconductor structure by forming a first source, a first drain, and a first gate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source, a second drain, and a second gate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source, a third drain, and a third gate;

forming a second pull-down transistor within the first semiconductor structure by forming a fourth source, a fourth drain, and a fourth gate;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; and

coupling the third source to the fourth contact and coupling the third contact to the first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

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80. The method of claim 79, further comprising:

doping the substrate to form a p-type conductivity; and

forming a n-type well within the first semiconductor structure.

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81. A method of fabricating a memory device comprising:

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure;

forming a second semiconductor structure;

forming a first pull-up transistor within the first semiconductor structure by forming a first source, a first drain, and a first gate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source, a second drain, and a second gate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source, a third drain, and a third gate;

forming a second pull-down transistor within the first semiconductor structure by forming a fourth source, a fourth drain, and a fourth;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; and

coupling the third source to the fourth contact and coupling the third contact to the first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.